REMARKS

Claims 32 through 39 and 44 through 53 are currently pending in the application.

This amendment is in response to the Office Action of July 2, 2002.

Claims 32 through 37, 39, 44 through 49 and 51 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan et al. (United States Patent 5,998,860) in view of Lin et al. (United States Patent 5,239,198).

Claims 32, 38, 44 and 50 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu (United States Patent 5,243,497) in view of Lin et al. (United States Patent 5,239,198).

Claims 35 through 37, 39, 47 through 49 and 51 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu in view of Lin et al., as applied to claims 32 and 44 above, and further in view of Chan et al.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants submit that the claimed invention is patentable over the cited prior art because the Examiner has not established a *prima facie* case of obviousness under 35 U.S.C. § 103.

Applicants submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. M.P.E.P. § 2143.

Claims 32 through 37, 39, 44 through 49 and 51 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan et al. in view of Lin et al. Applicants submit that there is no

suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine Chan et al. and Lin et al.

Chan et al. discloses using board-on-chip (BOC) type assembly of multiple semiconductor dice 50 on a printed circuit board 70. Further, Chan et al. uses wire bonds 80 to connect the semiconductor dice 50 to the opposing side of the substrate that semiconductor dice 50 are mounted to. The multiple semiconductor dice 50 mounted on printed circuit board 70 make up single inline memory module (SIMM) 20. SIMM 20 contains tabs 104 which are disposed on printed circuit board 70 "[t]o electrically connect to the expansion slot [on a motherboard of a personal computer]." (Chan et al., Column 4, Lines 58-60). Tabs 104 allow a fast and easy connection to a motherboard of a personal computer. Further, SIMM 20 is connected to a motherboard of a personal computer using only tabs 104 coupled to the mating connector on the motherboard of a personal computer. "Locating holes 102 are shown, which allow for the correct positioning of the double sided SIMM 20 of the present invention into, for example, an expansion slot." (Chan et al., Column 4, Lines 52-54). Therefore, SIMM 20 is not permanently connected to the motherboard of a personal computer, allowing for the memory of a personal computer to be easily increased to meet the memory demands of specific application programs.

Lin et al. discloses using chip-on-board (COB) type assembly of two semiconductor dice 10 mounted on a substrate 12 to form a multiple chip semiconductor device 10. Lin et al. uses wire bonds 22 or flip chip type bonding of semiconductor dice 10 to substrate 12. Multiple chip semiconductor device 10 is then soldered to a PC board using solder reflow methods "to securely affix the semiconductor device to the PC board." (Lin et al., Column 7, Lines 42-44). Therefore, Lin et al. discloses a permanent attachment of multiple chip semiconductor device 10 to a PC board.

Applicant submits that there is no motivation or suggestion to combine Chan et al. with Lin et al. Chan et al. contains no motivation or suggestion to modify its disclosure with the teachings of Lin et al. Further, Lin et al. contains no motivation or suggestion to modify its

disclosure with teachings of Chan et al. Chan et al. clearly teaches away from modifying its disclosure to use solder balls on its SIMM. The disclosure in Chan et al. only teaches non-permanently attaching SIMM 20 to a motherboard on a personal computer. Nothing in its disclosure suggests in anyway a permanent attachment to a motherboard as taught by Lin et al. and relied upon in the Office Action. Combining the teachings in such a way would change a principle of operation of the Chan et al. reference. "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." M.P.E.P. § 2143.01 (citing *In re Ratti* , 270 F.2d 810, 123 USPQ 349 (C.C.P.A. 1959). Similarly, if a "proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." M.P.E.P. § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)). The proposed combination would destroy the advantage of Chan et al., which is a SIMM that can be non-permanently attached to a motherboard on a personal computer.

The cited references of Chan et al. and Lin et al. further teach away from combining the references together due to the divergent ways that they mount semiconductor devices on a substrate. Chan et al. teaches using BOC type of mounting while Lin et al. teaches using COB type of mounting such as flip chip. There is no motivation or suggestion in Lin et al. to modify its disclosure to use the BOC type of mounting taught by Chan et al. and the claims of the present invention. In fact, Lin et al. teaches away from the proposed combination because it would lose the space saving advantages of COB type of mounting. Lin et al. teaches that by connecting semiconductor dice directly to a substrate, *i.e.* COB type of mounting, it "minimizes the area required by the [semiconductor] die and thus allows a very high substrate packing density." (Lin et al., Column 2, Lines 4-5). The Examiner is respectfully reminded that it "is improper to combine references where the references teach away from their combination." M.P.E.P. §2145(X)(D)(2) (citing *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)).

Therefore, the rejection of claims 32 through 37, 39, 44 through 49 and 51 as being unpatentable over Chan et al. and Lin et al. cannot stand since the combination is improper and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Claims 32, 38, 44 and 50 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu in view of Lin et al.. Applicants submit that there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine Chiu and Lin et al. to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Chiu discloses using board-on-chip (BOC) type assembly of multiple semiconductor chips 32 on a circuit board 31. Further, Chiu uses wire bonds 32a to connect the semiconductor chips 32 to the opposing side of the substrate that the semiconductor die is mounted to. The multiple semiconductor dice 32 mounted on circuit board 31 make up an assembly. Chiu is silent as to how the assembly will integrated or attached with higher level assemblies such as a motherboard on a personal computer.

As discussed previously, Lin et al. discloses using chip-on-board (COB) type assembly of two semiconductor dice 10 mounted on a substrate 12 to form a multiple chip semiconductor device 10. Lin et al. uses wire bonds 22 or flip chip type bonding of semiconductor dice 10 to substrate 12. Multiple chip semiconductor device 10 is then soldered to a PC board using solder reflow methods "to securely affix the semiconductor device to the PC board." (Column 7, Lines 42-44). Therefore, Lin et al. discloses a permanent attachment of multiple chip semiconductor device 10 to a PC board.

Applicant submits that there is no motivation or suggestion to modify Chiu to use the solder balls of Lin et al. to provide an input/output connection. Chiu is silent as to the method that it can be connected to higher level assemblies. Chiu contains no suggestion or motivation to incorporate the teachings of Lin et al. and any combination with Lin et al. is the result of impermissible hindsight reconstruction. The mere fact that references can be combined or

modified does not render the resultant combination obvious unless the prior art also suggests the combination. M.P.E.P. § 2143.01 (citing *In re Mills* , 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Even if the assembly of Chiu is capable of the proposed modification, there must be a suggestion or motivation in Chiu to do so.

Further, Applicant respectfully disagrees with the assertion in the Office Action that the assembly of Chiu will or can be connected to higher level assemblies by using solder balls on the wire bonded terminal contacts 34. (*See, Office Action*, July 2, 2002, page 7). Nothing in Chiu suggests that the terminal contacts 34 are large enough to support both a wire bond and a solder ball. Further, soldering over the wire bonds poses technical problems that are not discussed in any of the cited references.

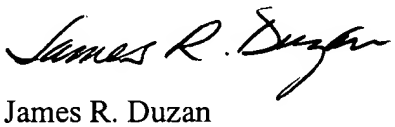
Even if there is a suggestion or motivation in the cited references or the knowledge commonly known in the art to modify Chiu to use solder balls of Lin et al. for an input/output connection, the cited references teach away from combining the references together due to the divergent ways that they mount semiconductor devices on a substrate. Chiu teaches using BOC type of mounting while Lin et al. teaches using COB type of mounting such as flip chip. There is no motivation or suggestion in Lin et al. to modify its disclosure to use the BOC type of mounting taught by Chiu and the claims of the present invention. In fact, Lin et al. teaches away from the proposed combination because it would lose the space saving advantages of COB type of mounting. Lin et al. teaches that by connecting semiconductor dice directly to a substrate, *i.e.* COB type of mounting, it "minimizes the area required by the [semiconductor] die and thus allows a very high substrate packing density." (Lin et al., Column 2, Lines 4-5). The Examiner is respectfully reminded that it "is improper to combine references where the references teach away from their combination." M.P.E.P. §2145(X)(D)(2) (citing *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)). Therefore, the rejection of claims 32, 38, 44 and 50 as being unpatentable over Chiu and Lin et al. cannot stand since there combination is improper and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Claims 35 through 37, 39, 47 through 49 and 51 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu in view of Lin et al., as applied to claims 32 and 44 above, and further in view of Chan et al. The above rejection cannot stand, as discussed above, since Lin et al. cannot be properly combined under 35 U.S.C. § 103(a) with either Chan et al. or Chiu because the references clearly teach away from any combination and cannot establish a *prima facie* case of obviousness under 35 U.S.C. §103 regarding the claimed invention. Also, since independent claim 32 and 44 are allowable, any claim depending from them are nonobvious. M.P.E.P. § 2143.03.

Applicants submit that claims 32 through 39 and 44 through 51 are clearly allowable over the cited prior art.

In summary, for the reasons set forth herein, Applicants request the allowance of claims 32 through 39 and 44 through 51 and the case passed for issue.

Respectfully submitted,



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